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EXAMINER	
NGUYEN, LEON VIET Q	
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2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,702	YU ET AL.	
	Examiner	Art Unit	
	Leon-Viet Q. Nguyen	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 11/08/2004 was filed after the mailing date of 11/08/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

1. Claim 11 objected to because of the following informalities:

   a. Claim 11 should read "signal delay circuitry, coupled to said high pass filter circuit, ***that*** delays..."

Appropriate correction is required.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-8, 15-21, and 24-29 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-32 of U.S. Patent No. 6,922,440 in view of U.S. Patent No. 4,970,703.

Re claim 1, "a first signal terminal that conveys a pre-decision data signal having a data symbol period associated therewith" corresponds to "a first signal terminal that conveys a pre-decision data signal having a data symbol period associated therewith"; "a second signal terminal that conveys an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency" corresponds to "a second signal terminal that conveys an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency"; "interpolating mixer circuitry, coupled to said first signal terminal, that receives and mixes an integrated signal and said pre-decision data signal to provide said adaptive signal, wherein said adaptive signal follows said pre-decision data signal by a second signal latency related to said first signal latency" corresponds to "adaptive timing interpolation circuitry, coupled to said first and second signal terminals, that receives said error signal and in response thereto receives

and adaptively processes said pre-decision data signal to provide said adaptive signal following said pre-decision data signal by a second signal latency related to said first signal latency; wherein said adaptive timing interpolation circuitry includes interpolating mixer circuitry, coupled to said first signal terminal, that receives and mixes an integrated signal and said pre-decision data signal to provide said adaptive signal"; "phase detection circuitry, coupled to said first and second signal terminals, that receives and detects a phase difference between said error signal and said pre-decision data signal to provide a detection signal" corresponds to "phase detection circuitry, coupled to said second signal terminal and said interpolating mixer circuitry, that receives and detects a phase difference between said error signal and said adaptive signal to provide a detection signal"; and "signal integration circuitry, coupled to said phase detection circuitry and said interpolating mixer circuitry, that receives and integrates said detection signal to provide said integrated signal" corresponds to "signal integration circuitry, coupled to said phase detection circuitry and said interpolating mixer circuitry, that receives and integrates said detection signal to provide said integrated signal" in claim 1 of U.S. Patent No. 6,922,440.

However claim 1 of U.S. Patent No. 6,922,440 fails to teach wherein the phase detection circuitry has a selected signal delay and wherein said selected signal delay is selected such that said integration signal has a substantially zero AC component.

U.S. Patent No. 4,970,703 teaches providing time delay for two stages (col. 2 lines 9-11, the time delay is interpreted to be the selected signal delay), which places the output of each stage at AC zero (col. 2 lines 12-14).

Therefore taking the combined teachings of U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the delay of U.S. Patent No. 4,970,703 into the apparatus of U.S. Patent No. 6,922,440. The motivation to combine U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 would be to provide DC stability and facilitate stage cascading (col. 2 lines 12-13).

Re claim 2, "fractional delay circuitry, coupled to said first signal terminal, that receives and delays said pre-decision data signal to provide a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period" corresponds to "fractional delay circuitry, coupled to said first signal terminal, that receives and delays said pre-decision data signal to provide a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period"; "signal weighting circuitry, coupled to said first signal terminal and said fractional delay circuitry, that receives said integrated signal and in response thereto receives and weights said pre-decision data signal and said delayed signal to provide first and second weighted signals" corresponds to "signal weighting circuitry, coupled to said first signal terminal and said fractional delay circuitry, that receives said integrated signal and in response thereto receives and weights said pre-decision data signal and said delayed signal to provide first and second weighted signals"; and "signal combining circuitry, coupled to said signal weighting circuitry, that receives and combines said first and second weighted signals to provide said adaptive signal"

corresponds to "signal combining circuitry, coupled to said signal weighting circuitry, that receives and combines said first and second weighted signals to provide said adaptive signal" in claim 1 of U.S. Patent No. 6,922,440.

Re claim 3, the limitations correspond to claim 2 of U.S. Patent No. 6,922,440.

Re claim 4, the limitations correspond to claim 3 of U.S. Patent No. 6,922,440.

Re claim 5, the limitations correspond to claim 4 of U.S. Patent No. 6,922,440.

Re claim 6, the limitations correspond to claim 5 of U.S. Patent No. 6,922,440.

Re claim 7, the limitations correspond to claim 6 of U.S. Patent No. 6,922,440.

Re claim 8, the limitations correspond to claim 7 of U.S. Patent No. 6,922,440.

Re claim 15, "signal receiving means for receiving" corresponds to "signal receiving means for receiving"; "a pre-decision data signal having a data symbol period associated therewith" corresponds to "a pre-decision data signal having a data symbol period associated therewith"; "an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency" corresponds to "an error signal

corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency"; "interpolating mixer means for receiving and mixing an integrated signal and said pre-decision data signal to generate said adaptive signal, wherein said adaptive signal follows said pre-decision data signal by a second signal latency related to said first signal latency" corresponds to "adaptive timing interpolator means for adaptively processing said pre-decision data signal in response to said error signal to generate said adaptive signal following said pre-decision data signal by a second signal latency related to said first signal latency; wherein said adaptive timing interpolator means includes interpolating mixer means for receiving and mixing an integrated signal and said pre-decision data signal to generate said adaptive signal"; "phase detector means for detecting a phase difference between said error signal and said pre-decision data signal to generate a detection signal" corresponds to "phase detector means for detecting a phase difference between said error signal and said adaptive signal to generate a detection signal"; and "signal integrator means for integrating said detection signal to generate said integrated signal" corresponds to "signal integrator means for integrating said detection signal to generate said integrated signal" in claim 16 of U.S. Patent No. 6,922,440.

However claim 16 of U.S. Patent No. 6,922,440 fails to teach wherein said selected signal delay is selected such that said integration signal has a substantially zero AC component.

U.S. Patent No. 4,970,703 teaches providing time delay for two stages (col. 2 lines 9-11, the time delay is interpreted to be the selected signal delay), which places the output of each stage at AC zero (col. 2 lines 12-14).

Therefore taking the combined teachings of U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the delay of U.S. Patent No. 4,970,703 into the apparatus of U.S. Patent No. 6,922,440. The motivation to combine U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 would be to provide DC stability and facilitate stage cascading (col. 2 lines 12-13).

Re claim 16, "fractional delay means for delaying said pre-decision data signal to generate a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period" corresponds to "fractional delay means for delaying said pre-decision data signal to generate a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period"; "signal weighting means for weighting said pre-decision data signal and said delayed signal in response to said integrated signal to generate first and second weighted signals" corresponds to "signal weighting means for weighting said pre-decision data signal and said delayed signal in response to said integrated signal to generate first and second weighted signals"; and "signal combiner means for combining said first and second weighted signals to generate said adaptive signal" corresponds to "signal

combiner means for combining said first and second weighted signals to generate said adaptive signal" in claim 16 of U.S. Patent No. 6,922,440.

Re claim 17, the limitations correspond to claim 17 of U.S. Patent No. 6,922,440.

Re claim 18, the limitations correspond to claim 18 of U.S. Patent No. 6,922,440.

Re claim 19, the limitations correspond to claim 19 of U.S. Patent No. 6,922,440.

Re claim 20, the limitations correspond to claim 20 of U.S. Patent No. 6,922,440.

Re claim 21, the limitations correspond to claim 21 of U.S. Patent No. 6,922,440.

Re claim 24, "receiving a pre-decision data signal having a data symbol period associated therewith" corresponds to "receiving a pre-decision data signal having a data symbol period associated therewith"; "receiving an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency" corresponds to "receiving an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency"; "receiving and mixing an integrated signal and said pre-decision data signal to generate said adaptive signal, wherein said

adaptive signal follows said pre-decision data signal by a second signal latency related to said first signal latency" corresponds to "wherein said receiving and adaptively processing said pre-decision data signal in response to said error signal to generate said adaptive signal following said pre-decision data signal by a second signal latency related to said first signal latency includes receiving and mixing an integrated signal and said pre-decision data signal to generate said adaptive signal"; "detecting a phase difference between said error signal and said pre-decision data signal to generate a detection signal" corresponds to "detecting a phase difference between said error signal and said adaptive signal to generate a detection signal"; and "integrating said detection signal to generate said integrated signal" corresponds to "integrating said detection signal to generate said integrated signal" in claim 28 of U.S. Patent No. 6,922,440.

However claim 28 of U.S. Patent No. 6,922,440 fails to teach wherein said selected signal delay is selected such that said integration signal has a substantially zero AC component.

U.S. Patent No. 4,970,703 teaches providing time delay for two stages (col. 2 lines 9-11, the time delay is interpreted to be the selected signal delay), which places the output of each stage at AC zero (col. 2 lines 12-14).

Therefore taking the combined teachings of U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the delay of U.S. Patent No. 4,970,703 into the apparatus of U.S. Patent No. 6,922,440. The motivation to combine

U.S. Patent No. 6,922,440 and U.S. Patent No. 4,970,703 would be to provide DC stability and facilitate stage cascading (col. 2 lines 12-13).

Re claim 25, "delaying said pre-decision data signal to generate a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period" corresponds to "delaying said pre-decision data signal to generate a delayed signal corresponding to and following said pre-decision data signal by a fraction of said data symbol period"; "weighting said pre-decision data signal and said delayed signal in response to said integrated signal to generate first and second weighted signals" corresponds to "said pre-decision data signal and said delayed signal in response to said integrated signal to generate first and second weighted signals"; and "combining said first and second weighted signals to generate said adaptive signal" corresponds to "combining said first and second weighted signals to generate said adaptive signal" in claim 28 of U.S. Patent No. 6,922,440.

Re claim 26, the limitations correspond to claim 29 of U.S. Patent No. 6,922,440.

Re claim 27, the limitations correspond to claim 30 of U.S. Patent No. 6,922,440.

Re claim 28, the limitations correspond to claim 31 of U.S. Patent No. 6,922,440.

Re claim 29, the limitations correspond to claim 32 of U.S. Patent No. 6,922,440.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15 and 24 recite the limitation "said selected delay signal". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1, 9, 12, 14-15, 22-24, and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi (US6201832).

Re claim 1, Choi discloses an apparatus including adaptive circuitry for introducing a compensating signal latency related to a signal latency of a data symbol decision circuit (fig. 2), comprising:

a first signal terminal that conveys a pre-decision data signal having a data symbol period associated therewith (Si in fig. 2);

a second signal terminal that conveys an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency (Ei-1 in fig. 2);

interpolating mixer circuitry (interpolation filter 20 in fig. 2), coupled to said first signal terminal (fig. 2), that receives and mixes an integrated signal and said pre-decision data signal to provide said adaptive signal, wherein said adaptive signal follows said pre-decision data signal by a second signal latency related to said first signal latency;

phase detection circuitry (phase error detector 70 in fig. 2), coupled to said first and second signal terminals (fig. 2) and having a selected signal delay (the delay from delay circuit 700 in fig. 9), that receives and detects a phase difference between said error signal and said pre-decision data signal to provide a detection signal (col. 14 lines 52-55); and

signal integration circuitry (loop filter 80 in fig. 2), coupled to said phase detection circuitry and said interpolating mixer circuitry (fig. 2), that receives and integrates said detection signal to provide said integrated signal, wherein said selected signal delay is selected such that said integrated signal has a substantially zero AC signal component (col. 15 lines 31-37, the predetermined analog voltage to the VCO circuit is interpreted to be *substantially* zero).

Re claim 9, Choi discloses an apparatus wherein said phase detection circuitry comprises:

signal differentiation circuitry (phase subtractor 640 in fig. 9), coupled to said first signal terminal and having said selected signal delay (delay from delay unit 464 in fig. 8), that differentiates and delays said pre-decision signal to provide a resultant signal (col. 15 lines 1-3), wherein respective portions of said resultant signal are delayed relative to corresponding portions of said pre-decision data signal by said selected signal delay (figs. 8 and 9, col. 14 lines 18-21); and

signal combining circuitry (multiplier 650 in fig. 9), coupled to said signal differentiation circuitry and said second signal terminal (fig. 9), that receives and combines said resultant signal and said error signal to provide said detection signal.

Re claim 12, Choi discloses an apparatus wherein said signal combining circuitry comprises signal multiplication circuitry that multiplies said resultant signal and said error signal to provide said detection signal (multiplier 650 in fig. 9).

Re claim 14, Choi discloses an apparatus further comprising signal combining circuitry (subtractor 55 in fig. 2), coupled to said interpolating mixer circuitry and said second signal terminal (fig. 2), that receives and combines said post-decision data signal and said adaptive signal to provide said error signal.

Re Claim 15, Choi discloses an apparatus including adaptive circuitry for introducing a compensating signal latency related to a signal latency of a data symbol decision circuit (fig. 2), comprising:

signal receiving means for receiving

a pre-decision data signal having a data symbol period associated therewith (Si in fig. 2), and

an error signal corresponding to a difference between an adaptive signal and a post-decision data signal which corresponds to and follows said pre-decision data signal by a first signal latency (Ei-1 in fig. 2);

interpolating mixer means for receiving and mixing an integrated signal and said pre-decision data signal to generate said adaptive signal (interpolation filter 20 in fig. 2), wherein said adaptive signal follows said pre-decision data signal by a second signal latency related to said first signal latency;

phase detector means for detecting a phase difference between said error signal and said pre-decision data signal to generate a detection signal (phase error detector 70 in fig. 2); and

signal integrator means for integrating said detection signal to generate said integrated signal(loop filter 80 in fig. 2), wherein said selected signal delay is selected such that said integrated signal has a substantially zero AC signal component.

Re claim 22, Choi discloses an apparatus wherein said phase detector means comprises:

signal differentiator means for differentiating and delaying said pre-decision signal to generate a resultant signal (phase subtractor 640 in fig. 9), wherein respective portions of said resultant signal are delayed relative to corresponding portions of said pre-decision data signal by said selected signal delay (figs. 8 and 9, col. 14 lines 18-21. Delay from delay unit 464 is interpreted to be said selected delay signal); and

signal combiner means for combining said resultant signal and said error signal to generate said detection signal (multiplier 650 in fig. 9).

Re claim 23, Choi discloses an apparatus further comprising signal combiner means for receiving and combining said post-decision data signal and said adaptive signal to generate said error signal (subtractor 55 in fig. 2).

Re claim 24, all of the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 15. It would be necessary to have a method for using the appartus as claimed in claim 15.

Re claim 30, all of the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 22.

Re claim 31, all of the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 23.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US6201832) as applied to claim 9 above, and further in view of Goldston et al (US20020012392).

Re claim 10, Choi fails to teach an apparatus wherein said signal differentiation circuitry comprises high pass filter circuitry that high pass filters and delays said pre-decision signal to produce said resultant signal. However Goldston teaches using highpass filter circuitry (filter 146 in fig. 2, ¶0022). Although not explicitly stated, it is well known to one of ordinary skill in the art that a filter causes some delay.

Therefore taking the combined teachings of Choi and Goldston as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the high pass filter of Goldston into the apparatus of Choi. The motivation to combine Goldston and Choi would be to eliminate the energy of an analog AM signal and provide a filtered signal (¶0022).

Re claim 11, Choi fails to teach an apparatus wherein said signal differentiation circuitry comprises: a high pass filter circuit that high pass filters said pre-decision signal to produce a high pass filtered signal; and signal delay circuitry, coupled to said high pass filter circuit, delays said high pass filtered signal to produce said resultant signal.

However Goldston teaches an apparatus wherein said signal differentiation circuitry comprises:

a high pass filter circuit (filter 146 in fig. 2, ¶0022) that high pass filters said pre-decision signal to produce a high pass filtered signal (148 in fig. 2); and

signal delay circuitry (delay circuit 168 in fig. 2), coupled to said high pass filter circuit (fig. 2), delays said high pass filtered signal to produce said resultant signal.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US6201832) as applied to claim 1 above, and further in view of Copeland (US6067319).

Re claim 13, Choi fails to teach an apparatus wherein said signal integration circuitry comprises low pass filter circuitry. However Copeland teaches the use of a low pass filter (LPF 914 in fig. 10).

Therefore taking the combined teachings of Choi and Copeland as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the low pass filter of Copeland into the apparatus of Choi. The motivation to combine Copeland and Choi would be to improve the SNR of the signal (col. 11 lines 55-62).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/

David C. Payne
DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER